INTL-0429-US
(P9135)

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: TILED DISPLAY

INVENTORS: DANIEL SELIGSON

Express Mail No.: EL732849866US

Date: March 28, 2001

TILED DISPLAY

Background

This invention relates generally to tiled displays.

Tiled displays may be made up of a plurality of display modules integrated by a plate such as a glass plate. Thus, the overall display image may be made up of subimages created by each of the display modules. By coordinating the display of subimages on each module, an overall coherent image may be generated.

Each of the individual modules may include a large number of pixels which are driven by drivers generally located remotely from those pixels. Because the tiled displays are generally made of material incompatible with logic devices, such as display drivers, the display drivers are formed in a surface separate from the actual display elements. This spacing of course adds to the complexity of the overall tiled display. The greater distance between the driver and the display may also adversely effect the speed of the display. Moreover, the need to interconnect the pixel elements with the drivers may increase the cost of the overall display.

Commonly, logic elements such as display drivers are formed of complementary metal oxide semiconductor (CMOS) integrated circuits. These devices can be fabricated at

low cost through high volume manufacturing procedures. In addition, the resulting devices are of extremely small size. Thus, the use of the CMOS integrated circuit fabrication techniques is generally preferred for making all types of logic devices including display drivers.

However, because of the basic incompatibility between the CMOS substrates and the substrates that are utilized in most display devices, a separate back plane must be provided on the display for mounting CMOS integrated circuits. These integrated circuits may then be connected from the back plane to the individual pixels or display elements. As mentioned above, this may result in reduced speed, increased cost, and overall complexity.

Some tiled displays use emissive display elements such as organic light emitting diodes. These displays use a passive matrix to drive the individual pixels. This has the advantage of reducing the cost, in particular the capital cost of the manufacturing infrastructure. However, a passive matrix drive (which is a form of multiplexing) puts extra demands on the emissive materials. When multiplexed, such materials are less efficient and have more reliability problems than when operated continuously.

Thus, there is a need for a way to make tiled displays in which the display drivers can be integrated into a display substrate.

Brief Description of the Drawings

Figure 1 is a partial, greatly enlarged perspective view of a trapezoidally-shaped block in position over a recessed region in a display substrate in accordance with one embodiment of the present invention;

Figure 2 is a partial plan view of the embodiment shown in Figure 1 after the block has been inserted into the substrate and the substrate and block have been planarized and metallized in accordance with one embodiment of the present invention;

Figure 3 is a top plan view of a portion of a tiled display in accordance with one embodiment of the present invention;

Figure 4 is a flow chart for fabricating one embodiment of the present invention;

Figure 5 is a top plan view of a tiled display in accordance with one embodiment of the present invention;

Figure 6 is a back plan view of one embodiment of the present invention;

Figure 7 is a greatly enlarged cross-sectional view through a portion of the tiled display shown in Figures 5 and 6;

Figure 8 is an enlarged view of a substrate utilized to form the trapezoidally-shaped blocks in accordance with one embodiment of the present invention;

Figure 9 shows a top plan view and side views of the masking process for forming the trapezoidally-shaped blocks in accordance with one embodiment of the present invention; and

Figure 10 is a schematic depiction of an apparatus for causing the trapezoidally-shaped blocks to enter recesses formed in a substrate in accordance with one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a trapezoidally-shaped complementary metal oxide semiconductor (CMOS) block 10, sometimes called a nanoblock, may include an upper surface 12 and angled or sloped side surfaces 14. The block 10 includes the CMOS driver circuits for driving a display element. The display element may be a liquid crystal display (LCD) element, an organic light emitting diode (OLED) or any of a variety of light emitting or non-light emitting display elements.

The block 10 is caused to enter a recessed region 18 in a substrate 16 that forms a tiled display. In some embodiments of the present invention, the substrate 16 may be a glass substrate conventionally utilized as the front plane in a tiled display. The tiled display substrate 16 may receive a very large number of blocks 10 to drive a very large number of display elements, each defining one or more pixels of an overall display.

After each block 10 has been appropriately positioned in a recessed region 18 in the substrate 16, appropriate thin film metallizations 20, shown in Figure 2, may be patterned over the substrate 16 and the block 10 to make electrical connections 24 to the various circuit components defined within the integrated circuits of the block 10. In one embodiment, the metallization 20 may be formed of a transparent conductor such as indium tin oxide. In addition, a passivation layer 22 may be provided over the block 10 and substrate 16. The metallization 20 and passivation layer 22 may effectively bind the block 10 to the substrate 16. However, as will be described in more detail hereinafter, other techniques may be utilized to further bind the block 10 and substrate 16.

Referring to Figure 3, a portion of the substrate 16 includes a plurality of pixel display elements 26. Each display element 26 may in turn create a set of colors associated with a known color space such as a red, green, blue (RGB) or YUV color spaces. Thus, each pixel color element 25 may selectively produce red, green or blue (or other colors). The individual pixel color element 25 corresponding to each color are driven by the circuitry included on the block 10. That is, each pixel color element 25 may be coupled to a driver 28 associated with the block 10 in one embodiment. In this way, each associated color may be independently driven.

In one embodiment of the present invention, the block 10 includes circuitry for driving a predetermined number, such as four, of display elements 26. As shown in Figure 3, the driven circuits included in the block 10 then may be positioned proximately to the very display elements 26 which the driving circuits are intended to drive. This advantageous arrangement may result in reduced cost and improved operating speed.

The drivers 28 are coupled to bond pads 30. The bond pads 30 then couple by vias (not shown) to other control circuits, such as video choppers or compensation logic as two examples, on a back plane (not shown in Figure 3).

Turning next to Figure 5, the overall tiled display 11 may include a frame 14 and a optical integrator 46 which may be formed of a glass plate as one example. The front plane substrate 16, shown in Figure 6, may include a plurality of display modules 48 separated by joints 50. The display modules 48 collectively form subimages of the overall image visible from the front plane or substrate 16.

Referring to Figure 4, an overview of the process of fabricating the blocks 10 and depositing them into the substrate 16 is depicted. Initially, the substrate 16 is prepared as indicated in block 32. The nanoblock receiving regions 18 are etched into the substrate 16 as indicated in block 34. The blocks 10 are then deposited as indicated in block 36. The blocks 10 then may be bonded to the

substrate 16 as indicated in block 38. Thereafter, the pixels 25 may be defined as indicated in block 40 and the overall structure may be passivated and metallized as indicated in block 42.

Thus, referring to Figure 7, the block 10 sits within the recessed region 18 of the front plane or substrate 16. The back plane 47 may include integrated control circuits that couple by vias (not shown) to the blocks 10. An optical integrator 46 may integrate a plurality of modules 48. The images generated by the pixel color elements 25 may be viewed from the substrate 16 in accordance with one embodiment of the present invention.

The block 10 may be formed in a substrate 52, such as a silicon wafer, that has a bottom surface 56 and an upper surface 54, as shown in Figure 8. Bottom surface 56 is the polished side of silicon wafer 52, and upper surface 54 is the unpolished, rough side. A sacrificial layer 58 overlying upper surface 56, may be formed by chemical vapor deposition, sputtering, molecular beam epitaxy, or the like.

Sacrificial layer 58 is a layer made of silicon nitride (SiN_x), silicon dioxide SiO_2, metals, or organics, with a thickness of about 100 Å to about 100 μm, such as a SiN_x layer of about 0.4 μm thickness. Masking and etching steps can be used to form the trapezoidally-shaped blocks 10. In this embodiment, a trapezoidally-shaped block 10

includes a base with four sides protruding therefrom to a larger top surface. Each side creates an angle between about 20° and about 90° from the top surface to a side, and may be about 55° in one embodiment. The block may have a length between about 1 μm and about 1 cm, and a width between about 1 μm and about 1 cm, and may have a length of about 1.0 mm and a width of about 1.2 mm in one embodiment. The larger face is on, and in contact with, the sacrificial layer 58. A subsequent step of preferential etching removes sacrificial layer 58 to free each trapezoidally-shaped block 10 formed overlying sacrificial layer 58. The blocks 10 are then transferred into a fluid to form a slurry.

The slowest etching planes for silicon in a $KOH:H_2O$ etching solution are the {111} planes, which can be considered etch stops forming the sloping sides of the shaped blocks 10. The respective mask used to define the blocks is aligned to the appropriate crystal axis. As shown in Figure 9, a mask 60 forms the silicon trapezoidally-shaped blocks 10. Silicon trapezoidally-shaped block 10 is formed at the intersection of the diagonal lines on mask 60, and the larger face 61 of silicon trapezoidally-shaped block 10 is in contact with sacrificial layer 62. The width of the diagonal mask lines may be twice the thickness (t) of silicon block layer. In one embodiment, a=0.2 mm and silicon layer 52 has t=235 μm.

Etching is completed when silicon layer 52 is etched entirely through, and simultaneously when the corners are precisely formed. Continuing etching beyond this point does not change the overall dimensions of the trapezoidally-shaped block 10, but merely rounds the corners. Because of geometric considerations, the width of the top face of the shaped block 10 may be at least $3\sqrt{2}$ times the thickness of the silicon layer 52. This limits the aspect ratio of the blocks fabricated by the this technique. This mask pattern utilizes as much as 50% of the silicon area if there is no distance between block corners.

The etched silicon wafer is placed in concentrated hydrofluoric (HF) etch solution to remove the shaped blocks from contact with the SiN_x sacrificial layer 58 and any remaining SiN_x from the mask layer. This HF etch solution preferentially etches the sacrificial layer 58 to free the shaped blocks without etching the shaped blocks. In particular, an HF solution having a concentration of about 1:1 $HF:H_2O$ may be used to etch the sacrificial layer 58 to free the shaped blocks 10 without etching the silicon shaped blocks 10.

The slurry comprises an inert solution of fluid and shaped blocks. Enough solution exists in the slurry to allow the blocks to slide across the top surface of a substrate. Preferably, the amount of solution in the

mixture is at least the same order as the amount of blocks. Of course, the amount of solution necessary depends upon characteristics such as block size, block material, substrate size, substrate materials, and solution.

The glass tiled display substrate 16 may have etched recessed regions 18 as shown in Figure 1. A variety of techniques including wet etching, plasma etching, reactive ion etching, ion milling, among others provide recessed regions 18, or generally trenches, receptors, or binding sites. Such techniques etch recessed regions 18 with a geometric profile which is complementary to the block 10. In the glass substrate 16, for example, each recessed region 18 includes a trapezoidal profile or inverted truncated pyramid shape. The trapezoidal profile allows block 10 to self-align and fit closely into recessed region 18 via a transferring technique.

The transferring technique includes evenly spreading or pouring the slurry over the substrate 16. The slurry may be transferred from any type of vessel and/or apparatus capable of evenly transferring the slurry over substrate 16. Generally, the slurry is poured over top of the substrate 16 at a rate which allows substantial coverage, but prevents blocks 10 already disposed into the recessed regions 18 from floating or popping out. Slurry flow is typically laminar but can be non-laminar, depending upon the particular application. The blocks 10 flow evenly with

the fluid, tumble onto the substrate 16, self-align, and settle into recessed regions 18.

Optionally, to prevent the blocks already disposed in the recessed regions from floating out, the transferring step may take place in a centrifuge or the like. A centrifuge, for example, places a force on the blocks 10 already disposed in the recessed regions and thereby prevents such blocks from floating out with solution.

As illustrated in Figure 10, an apparatus 70 includes a vessel 72 and a pump 74. Vessel 72 includes a receptacle 76 and a conduit 78. Vessel 72 contains a substrate 16 having recessed regions 18 receiving the mixture of fluid and shaped blocks 10. Conduit 78, coupled to receptacle 70 which contains substrate 16, includes an input 82, an output 84 leading back to receptacle 76, and a column 86 coupled to one end of input 82 and at the other end to output 76. Pump 74 is coupled to input 82 and dispenses a gas into conduit 78 to facilitate circulation of the fluid and shaped blocks over substrate 16 at a rate where at least one shaped block 10 is disposed into a recessed region 18.

Receptacle 76 includes a holder 90 and a funneled bottom 92. Holder 90 secures substrate 16 and is capable of moving substrate 16 to facilitate the filling of the recessed regions 18. Additionally, holder 90 agitates or orients substrate 16 so that shaped blocks 10 not disposed

in recessed regions 18 can flow off substrate 16 and back into a recirculation path in vessel 92. The bottom of receptacle 76 is funnel-shaped to cause the shaped blocks 10 not disposed into recessed regions on substrate 16 to fall to the bottom of receptacle 76 for recirculation through vessel 72. Shaped blocks not disposed into recessed regions then recirculate through vessel 72.

More specifically, funnel bottom 72 is coupled to input 82 of conduit 72. Shaped blocks 10 not disposed into recessed regions 18 tumble to funneled bottom 92 to input 82 of conduit 70, where pump 74 dispenses as gas, such as nitrogen. The injected gas forms bubbles within the fluid inside column 86. A gas bubble transports a portion of the fluid and at least one shaped block funneled to input 82 through column 86 back to receptacle through output 84 for attempted disposition into a recessed region. The gas bubble rises through column 86 and transports the fluid and the shaped block to output 84 leading back to receptacle 76.

In this embodiment, apparatus 70 uses nitrogen bubbles to circulate the fluid and the shaped blocks over substrate 16 without damaging the shaped blocks. Depending on, among other factors, the material of the shaped blocks and the fluid used, apparatus 70 may use other media, or gases such as air, hydrogen (H_2), nitrogen (N_2), oxygen (O_2), or argon (Ar) which do not damage the blocks or otherwise react with the fluid. Pump 74 dispenses the gas or transport medium

which can be changed to achieve different fill-factors of the recessed regions.

In a modification to the preceding specific embodiment, the blocks 10 are attached into recessed regions 18 through eutectic layer. Prior to the lift-off step, a metallized layer such as gold, silver, solder, or the like is formed over the regions 18. Alternatively, the layer attaching the block 10 with each recessed region 18 may be a synthetic adhesive or the like instead of a eutectic layer. Process steps comprising masking, etching, and sputtering typically form such metallized layer. Subsequent to the transferring step, a heating structure forms a eutectic layer between metallization layer and silicon substrate 16.

Bubbles may stick to the shaped blocks 10 and to the recessed regions 18 due to the fact that all the silicon surfaces are hydrophobic. Adding a small amount of surfactant makes the silicon surfaces less hydrophobic. The substrate 16 may be oriented at an angle which causes the incorrectly oriented blocks to slide off. Agitation and correct orientation of the substrate 16 may increase the rate at which the blocks fill the regions 18.

In some embodiments, the blocks 10 may include active display drivers which continuously drive the individual pixels. Continuously driving the pixels from the front plane may reduce the demands on emissive materials compared

to passive matrix drive systems wherein the pixels are driven in a multiplexing system from the back plane.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: